Opcode Tables

Major Opcode (inst. bits 0 to 5)

	x0	x1	x2	x3	x4	x5	x6	x7	x8	x9	xA	xB	xC	xD	xE	xF
0x	BRK	{FVECTOR}	{R2}	AUIPC	ADDI	CSR	SLTI	SLTUI	ANDI	ORI	XORI		BLEND	REX	XNORI	{FLOAT}
1x		LVxU		LB		SB	{MNDX}	SWC	JAL	CALL	INC / DEC	LFx	SGTUI	LWR	CACHE	EXEC
2x	LC / LH / LW / LD	LCU / LHU	{BITFIELD}	LBU	SC / SH / SW	CAS	BBC / BBS	LUI	JMP	RET	MULFI	SFx	SGTI	{CMPRSSD}	MODI	{AMO}
3x	Bcc	{IVECTOR}	BEQ#	BCHK	CHK		LV	SV	MULUI	FXMULI	MULI	LVx	DIVUI	NOP	DIVI	{AMO}

Memory Indexed (inst. bits 21,22,28 to 31) (or bits 16,17, 28 to 31 for stores) (bit 31 = 0 for loads, 1 for stores)

	x0	x1	x2	x3	x4	x5	x6	x7	x8	x9	xA	xB	xC	xD	xE	xF
0x	LVBX	LVBUX	LVCX	LVCUX	LVHX	LVHUX	LVWX		LCX	LCUX	LBUX					
1x	LHX	LHUX	LWX	LBX	LWRX				LVWS	LVX		LFHX	LFSX	LFDX	CACHEX	LFQX
2x	SBX	SHX	SWX	SWCX	SCX	CASX		SVWS			INCX / DECX	SFHX	SFSX	SFDX		SFQX
3x				PUSH				SVX								

Major Funct (inst. bits 26 to 31)

	x0	x1	x2	x3	x4	x5	x6	x7	x8	x9	xA	xB	xC	xD	xE	xF
0x	{BCD}	{R1}	ADDV	BMM	ADD	SUB	SLT	SLTU	AND	OR	XOR	SUBV	NAND	NOR	XNOR	{shift31}

1x		TRANSFORM			MODU	MODSU	MOD		LEAX		INCX		MOV		PTRDIF	{shift63}
2x	TESTSCN	TEST_CLIP	MOV	MOV	MULUH	MULSUH	MULH		SLE	SLEU	MULF	FXDIV	MIN	MAX	MAJ	{shiftr}
3x	SEI / CLI	WAIT	RTI	VMOV	CHK	SLE	{SEG}		MULU	MULSU	MUL	FXMUL	DIVU	DIVSU	DIV	TLB

Major Funct (inst. bits 42 to 47)

	x0	x1	x2	x3	x4	x5	x6	x7	x8	x9	xA	xB	xC	xD	xE	xF
0x	RTOP	{R1}	ADDV		ADD	SUB			AND	OR	XOR	SUBV	NAND	NOR	XNOR	{shift31}
1x												MUX	MOV			{shift63}
2x			MOV					CMOVFNZ	CMOVEZ	CMOVNZ			MIN3	MAX3	MAJ	{shiftr}
3x									MULU	MULSU	MUL		DIVMODU	DIVMODSU	DIVMOD	

Float Funct (inst. bits 26 to 31)

	x0	x1	x2	x3	x4	x5	x6	x7	x8	x9	xA	xB	xC	xD	xE	xF
0x					FADD	FSUB	FCMP		FMUL	FDIV						
1x	FMOV		FTOI	ITOF	FNEG	FABS	FSIGN	FMAN	FNABS	FCVTSD		FCVTSQ	FSTAT	FSQRT		
2x	FTX	FCX	FEX	FDX	FRM					FCVTDS						
3x							FSYNC		FSLT	FSGE	FSLE	FSGT	FSEQ	FSNE	FSUN	

R1 (inst. bits 21 to 25)

	x0	x1	x2	x3	x4	x5	x6	x7	x8	x9	xA	xB	xC	xD	xE	xF
0x	CNTLZ	CNTLO	CNTPOP	COM	ABS	NOT	REDOR	NEG	ZXH	ZXC	ZXB	4to8	2to8		POPR	
1x	MEMDB	MEMSB	SYNC		CHAIN OFF	CHAIN ON	SETWB		SXH	SXC	SXB	8to4	8to2			RD_CMD_COUNT

Shift (inst. bits 22 to 25)

	x0	x1	x2	x3	x4	x5	x6	x7	x8	x9	xA	xB	xC	xD	xE	xF
0x	SHL	SHR	ASL	ASR	ROL	ROR			SHLI	SHRI	ASLI	ASRI	ROLI	RORI		

Vector Funct (inst. bits 26 to 31)

	x0	x1	x2	x3	x4	x5	x6	x7	x8	x9	xA	xB	xC	xD	xE	xF
0x	VCMPRSS	VCIDX	VSCAN	VABS	VADD	VSUB	VSxx	VSxxS	VAND	VOR	VXOR	VXCHG	VSHL	VSHR	VASR	
1x	VSHLV	VSHRV			VADDS	VSUBS	VSUBRS	VSxxSU	VANDS	VORS	VXORS					
2x	VBITS2V	V2BITS	VEINS / VMOVSV	VEX / VMOVS	VFLT2INT	VINT2FLT	VSIGN	VSxxU	VCNTPOP		VMULS				VDIVS	
3x	VMAND	VMOR	VMXOR	VMXNOR	VMPOP	VMFILL	VMFIRST	VMLAST			VMUL				VDIV	